Listing of Claims:

1. (CURRENTLY AMENDED) An active pixel sensor, comprising:

a p type epitaxial silicon substrate;

an N well formed in said substrate;

a P well formed in said N well;

a deep N well formed in said substrate beneath said P well wherein charge is accumulated by said deep N well during a charge integration period;

an overlap region formed between said N well and said deep N well wherein said overlap region is ~~designed such that the potential of said P well can cause said overlap region to be depleted or not depleted of charge carriers and said overlap region is~~ depleted of charge carriers and thereby electrically isolates said N well from said deep N well preventing charge transfer between said deep N well and said N well during said charge integration period and is not depleted of charge carriers and thereby electrically connects said N well to said deep N well enabling charge transfer between said deep N well and said N well after said charge integration period has been completed;

a first N region and a second N region formed in said P well; and

a P region formed in said N well.

2. (ORIGINAL) The active pixel sensor of claim 1 wherein said first N region and said second N region provide electrical communication to said P well and said P region provides electrical communication to said N well.

3. (ORIGINAL) The active pixel sensor of claim 1 wherein the potential of said P well and the potential of said N well determine whether or not said overlap region is depleted of charge carriers or is not depleted of charge carriers.

4. (ORIGINAL) The active pixel sensor of claim 1 wherein said first N region, said second N region, and said P well can be used to form a floating gate field effect transistor.

5. (PREVIOUSLY PRESENTED) The active pixel sensor of claim 1 wherein the potential of said P well is set so that said overlap region is depleted of charge carriers during said charge integration period.

6. (PREVIOUSLY PRESENTED) The active pixel sensor of claim 1 wherein the potential of said P well is set so that said overlap region is not depleted of charge carriers after said charge integration period has been completed.

7. (PREVIOUSLY PRESENTED) The active pixel sensor of claim 1 wherein the potential of said P well is set so that said overlap region is not depleted of charge carriers after said charge integration period has been completed and said first N region, said second N region, and said P well are used as a floating gate field effect transistor.

8. (CURRENTLY AMENDED) An array of active pixel sensors comprising:

a p type epitaxial silicon substrate;

a number of N wells formed in said substrate;

a P well formed in each of said N wells;

a deep N well formed in said substrate wherein said deep N well extends beneath each of said P wells and said deep N well accumulates charge during a charge integration period;

an overlap region formed between each of said N wells and said deep N well wherein said each of said overlap regions are ~~designed such that the potential of said P wells can cause said overlap regions to be depleted or not depleted of charge carriers and said overlap regions are~~ depleted of charge carriers and thereby electrically isolate each of said N wells from said deep N well preventing charge transfer between said deep N well and said N wells during said charge integration period and selected overlap regions are not depleted of charge carriers and thereby electrically connect selected said N wells to said deep N well enabling charge transfer between said deep N well and selected said N wells after said charge integration period has been completed;

a first N region and a second N region formed in each of said P wells; and

a P region formed in each of said N wells.

9. (ORIGINAL) The array of claim 8 wherein said first N region and said second N region in each of said P wells provide electrical communication to that said P well.

10. (ORIGINAL) The array of claim 8 wherein said P region formed in each of said N wells provides electrical communication to that said N well.

11. (ORIGINAL) The array of claim 8 wherein for each of said N wells the potential of that said N well and the potential of said P well in that said N well determines whether or not said overlap region between that said N well and said deep N well is depleted of charge carriers or is not depleted of charge carriers.

12. (ORIGINAL) The array of claim 8 wherein for each of said N wells said P well in that said N well, said first N region in said P well in that said N well, and said second N region in said P well in that said N well can be used to form a floating gate field effect transistor in that said N well.

13. (ORIGINAL) The array of claim 8 wherein the potentials of each of said P wells are set so that said overlap regions between each of said N wells and said deep N well are not depleted of charge carriers during a reset cycle.

14. (ORIGINAL) The array of claim 8 wherein a selected group of said N wells can be binned together by setting the potentials of each of said P wells in said selected group of said N wells so that said overlap regions between each of said N wells in said selected group of said N wells and said deep N well are not depleted of charge.

15. (PREVIOUSLY PRESENTED) The array of claim 8 wherein the potentials of each of said P wells are set so that said overlap regions between each of said N wells and said deep N well are depleted of charge carriers during said charge integration period.

16. (PREVIOUSLY PRESENTED) The array of claim 8 wherein the potentials of each of said P wells are set so that said overlap regions between each of said N wells and said deep N well are not depleted of charge carriers after said charge integration period has been completed.

17. (PREVIOUSLY PRESENTED) The array of claim 8 wherein the potentials of each of said P wells are set so that said overlap regions between each of said N wells and said deep N well are not depleted of charge carriers after said charge integration period has been completed and said first N region, said second N region, and said P well in each of said N wells are used as a floating gate field effect transistor.

18. (CURRENTLY AMENDED) An active pixel sensor, comprising:

an n type epitaxial silicon substrate;

a P well formed in said substrate;

an N well formed in said P well;

a deep P well formed in said substrate beneath said N well wherein charge is accumulated by said deep P well during a charge integration period;

an overlap region formed between said P well and said deep P well wherein said overlap region is ~~designed such that the potential of said N well can cause said overlap region to be depleted or not depleted of charge carriers and said overlap region is~~ depleted of charge carriers and thereby electrically isolates said P well from said deep P well preventing charge transfer between said deep P well and said P well during said charge integration period and is not depleted of charge carriers and thereby electrically connects said P well to said deep P well enabling charge transfer between said deep P well and said P well after said charge integration period has been completed;

a first P region and a second P region formed in said N well; and

an N region formed in said P well.

19. (ORIGINAL) The active pixel sensor of claim 18 wherein said first P region and said second P region provide electrical communication to said N well and said N region provides electrical communication to said P well.

20. (ORIGINAL) The active pixel sensor of claim 18 wherein the potential of said N well and the potential of said P well determine whether or not said overlap region is depleted of charge carriers or is not depleted of charge carriers.

21. (ORIGINAL) The active pixel sensor of claim 18 wherein said first P region, said second P region, and said N well can be used to form a floating gate field effect transistor.

22. (PREVIOUSLY PRESENTED) The active pixel sensor of claim 18 wherein the potential of said N well is set so that said overlap region is depleted of charge carriers during said charge integration period.

23. (PREVIOUSLY PRESENTED) The active pixel sensor of claim 18 wherein the potential of said N well is set so that said overlap region is not depleted of charge carriers after said charge integration period has been completed.

24. (PREVIOUSLY PRESENTED) The active pixel sensor of claim 18 wherein the potential of said N well is set so that said overlap region is not depleted of charge carriers after said charge integration period has been completed and said first P region, said second P region, and said N well are used as a floating gate field effect transistor.

25. (CURRENTLY AMENDED) An array of active pixel sensors comprising:

an n type epitaxial silicon substrate;

a number of P wells formed in said substrate;

an N well formed in each of said P wells;

a deep P well formed in said substrate wherein said deep P well extends beneath each of said N wells and said deep P well accumulates charge during a charge integration period;

an overlap region formed between each of said P wells and said deep P well wherein said each of said overlap regions are ~~designed such that the potential of said N well can cause said overlap regions to be depleted or not depleted of charge carriers and said overlap regions are~~ depleted of charge carriers and thereby electrically isolate each of said P wells from said deep P well preventing charge transfer between said deep P well and said P wells during said charge integration period and selected overlap regions are not depleted of charge carriers and thereby electrically connect selected said P wells to said deep P well enabling charge transfer between said deep P well and selected said P wells after said charge integration period has been completed;

a first P region and a second P region formed in each of said N wells; and

an N region formed in each of said P wells.

26. (ORIGINAL) The array of claim 25 wherein said first P region and said second P region in each of said N wells provide electrical communication to that said N well.

27. (ORIGINAL) The array of claim 25 wherein said P region formed in each of said P wells provides electrical communication to that said P well.

28. (ORIGINAL) The array of claim 25 wherein for each of said P wells the potential of that said P well and the potential of said N well in that said P well determines whether or not said overlap region between that said P well and said deep P well is depleted of charge carriers or is not depleted of charge carriers.

29. (ORIGINAL) The array of claim 25 wherein for each of said P wells said N well in that said P well, said first P region in said N well in that said P well, and said second P region in said N well in that said P well can be used to form a floating gate field effect transistor in that said P well.

30. (ORIGINAL) The array of claim 25 wherein the potentials of each of said N wells are set so that said overlap regions between each of said P wells and said deep P well are not depleted of charge carriers during a reset cycle.

31. (ORIGINAL) The array of claim 25 wherein a selected group of said P wells can be binned together by setting the potentials of each of said N wells in said selected group of said P wells so that said overlap regions between each of said P wells in said selected group of said P wells and said deep P well are not depleted of charge.

32. (PREVIOUSLY PRESENTED) The array of claim 25 wherein the potentials of each of said N wells are set so that said overlap regions between each of said P wells and said deep P well are depleted of charge carriers during said charge integration period.

33. (PREVIOUSLY PRESENTED) The array of claim 25 wherein the potentials of each of said N wells are set so that said overlap regions between each of said P wells and said deep P well are not depleted of charge carriers after said charge integration period has been completed.

34. (PREVIOUSLY PRESENTED) The array of claim 25 wherein the potentials of each of said N wells are set so that said overlap regions between each of said P wells and said deep P well are not depleted of charge carriers after said charge integration period has been completed and said first P region, said second P region, and said N well in each of said P wells are used as a floating gate field effect transistor.